CLAIMS

What is claimed is:

> [Note: Square bracketed and small-sized cross-referencing text is provided in the below application claims as an aid for readability and for finding corresponding (but not limiting) examples of support in the specification. The bracketed text (e.g., [100] is not intended to add any limitation whatsoever to the claims and should be deleted in all legal interpretations of the claims and should also be deleted from the final published version of the claims.]

1. A field programmable gate array (FPGA) [200] comprising:

(a) a plurality of logic blocks [250] organized as rows and columns;

(b) a plurality of horizontal and vertical interconnect channels (HIC's and VIC's) [402,401] extending respectively along the rows and columns of said logic blocks for providing interconnection between the logic blocks;

(c) at least first and second columns [223-224] of configurable memory blocks (CMB's) [210,310] embedded among the columns of logic blocks, wherein:

(c.1) each CMB spans a plurality of said HIC's [261-264];

(c.2) each given CMB has plural data-I/O sub-busses [314a-314d], operatively coupled to a different one of the HIC's among the HIC's spanned by the given CMB;

(c.3) each given CMB is programmably configurable into at

least a respective shallow-and-wide mode in which data-I/O words of the CMB have a relatively large, first number of bits per word and a correspondingly relatively large first number of said data-I/O sub-busses are used for conducting in parallel, the bits of the data-I/O words in the respective shallow-and-wide mode; and

(c.4) each given CMB is further programmably configurable at least into a respective deep-and-narrow mode in which data-I/O words of the CMB have a relatively small second number of bits per word and a correspondingly relatively small second number of said data I/O sub-busses are used for conducting in parallel, the bits of the data-I/O words in the respective deep-and-narrow mode, where the relatively small second number of the respective deep-and-narrow mode is less than the corresponding relatively large, first number of the respective shallow-and-wide mode.

2. The FPGA of Claim 1 and further wherein:

(c.5) CMB's [214'-215'] which span same HIC's but occupy different columns can be configured into complementary deep-and-narrow modes wherein, if a first data-I/O sub-bus [314c] of a corresponding first CMB [310] is unusable because the first CMB is in a respective first deep-and-narrow mode, a complementary second data-I/O sub-bus [314c'] of a corresponding second CMB [310'] in a

different column is usable for conducting data of the given HIC to which the unusable first data-I/O sub-bus couples, where the second data-I/O sub-bus also couples to the given HIC [305c].

3. The FPGA of Claim 1 wherein said relatively large number of bits of each respective shallow-and-wide mode is at least sixteen.

4. The FPGA of Claim 3 wherein said relatively small number of bits of each deep-and-narrow mode is less than ten but greater than zero.

5. The FPGA of Claim 3 wherein each respective deep-and-narrow mode provides for random addressing of at least 512 data words in each respective CMB.

6. The FPGA of Claim 1 wherein each CMB has at least two independently usable ports [Port-0,Port-1] structured to receive respectively independent address signals [312] and to independently read from, or write to, respectively addressed data word storage locations of the CMB.

7. The FPGA of Claim 1 and further comprising:

(d) at least third and fourth columns [225-226] of said CMB's embedded among the columns of logic blocks, wherein:

(d.1) the FPGA is divided into plural partitions with the first and second columns of said CMB's occupying a first [201] of the partitions, with the third and fourth columns of said CMB's occupying a second [202] of the partitions, the second partition being horizontally separated [207] from the first partition; and the FPGA further having:

(e) horizontal joiners [270-279] for programmably joining and disjoining interconnect resources of the first and second partitions.

8. The FPGA of Claim 6 wherein:

said sub-busses of the CMB's couple to longline segments in the respective partitions of the CMB's; and

said horizontal joiners [270-279] include programmable tri-state buffers [575,577] for programmably joining longline segments of the first partition with corresponding longline segments of the second partition.

9. A method for configuring a field programmable gate array (FPGA) [200], where the FPGA includes:

(0.1) a plurality of logic blocks [250] organized as rows and columns;

(0.2) a plurality of horizontal and vertical interconnect channels (HIC's and VIC's) [402,401] extending respectively along the rows and columns of said logic blocks for providing interconnection between the logic blocks;

(0.3) at least first and second columns [223-224] of configurable memory blocks (CMB's) [210,310] embedded among the columns of logic blocks, wherein:

(0.3a) each CMB spans a plurality of said HIC's [261-264];

(0.3b) each given CMB has plural data-I/O sub-busses [314a-314d], operatively coupled to a different one of the HIC's among the HIC's spanned by the given CMB;

(0.3c) each given CMB is programmably configurable into at least a respective first shallow-and-wide mode in which data-I/O words of the CMB have a pre-defined, relatively large number of bits per word and a correspondingly, relatively large number of said data-I/O sub-busses are used for conducting in parallel, the bits of the data-I/O words in the respective, first shallow-and-wide mode; and

(0.3d) each given CMB is further programmably configurable into a respective deep-and-narrow mode in which data-I/O words of the CMB have a pre-defined, relatively small number of bits per word and a correspondingly relatively small number of said data I/O sub-busses are used for conducting in parallel, the bits of the data-I/O words in the respective deep-and-narrow mode, the relatively small number of bits per word of each respective CMB being smaller than the relatively large number of bits per word of the respective CMB;

said configuring method comprising:

(a) configuring CMB's [214'-215'] which span same HIC's but respectively occupy different columns into respective complementary deep-and-narrow modes wherein, when a first data-I/O sub-bus [314c] of a corresponding first CMB [310] becomes unusable because the first CMB is configured into a first deep-and-narrow mode, the configuring causes a complementary second data-I/O sub-bus [314c'] of a corresponding second CMB [310'] in a different column to become usable for conducting data of the given HIC to which the unusable first data-I/O sub-bus couples, where the second data-I/O sub-bus also couples to the given HIC [305c].

10. A field programmable gate array (FPGA) [200] comprising:

(a) a plurality of logic blocks [250] organized as rows and columns;

(b) a plurality of horizontal and vertical interconnect channels (HIC's and VIC's) [402,401] extending respectively along the rows and columns of said logic blocks for providing interconnection between the logic blocks;

(c) a plurality of configurable memory blocks (CMB's) [210,310] embedded among the columns of logic blocks, wherein:

(c.1) each CMB spans a plurality of said HIC's [261-264];

(c.2) each given CMB has plural data-I/O sub-busses [314a-314d], operatively coupled to a different one of the HIC's among the

HIC's spanned by the given CMB; and

wherein each CMB has at least two independently usable ports [Port-0,Port-1] structured to receive respectively independent address signals [312] and to independently read from, or write to, respectively addressed data word storage locations of the CMB.

11. The FPGA of claim 10 wherein

(c.3) each given CMB is programmably configurable into at least a first mode in which data-I/O words of the CMB have a larger number of bits per word and a correspondingly larger number of said data-I/O sub-busses are used for conducting in parallel, the bits of the data-I/O words in the first mode; and

(c.4) each given CMB is further programmably configurable into a second mode in which data-I/O words of the CMB have a smaller number of bits per word and a correspondingly smaller number of said data I/O sub-busses are used for conducting in parallel, the bits of the data-I/O words in the second mode.